



# STD100N03L STD100N03L-1

N-channel 30V - 0.0045Ω - 80A - DPAK - IPAK  
Planar STripFET™ II Power MOSFET

## General features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>	P <sub>w</sub>
STD100N03L	30 V	<0.0055 Ω	80 A <sup>(1)</sup>	110 W
STD100N03L-1	30 V	<0.0055 Ω	80 A <sup>(1)</sup>	110 W

1. Current limited by package

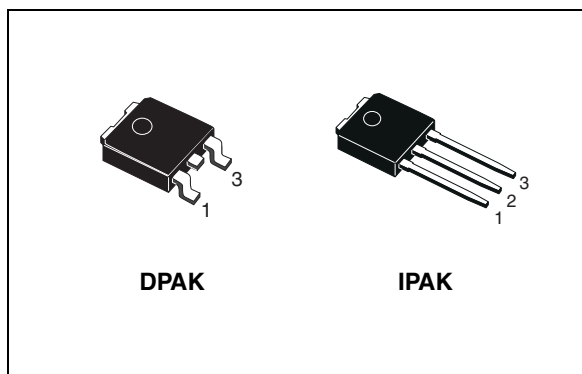
- 100% avalanche tested
- Logic level threshold

## Description

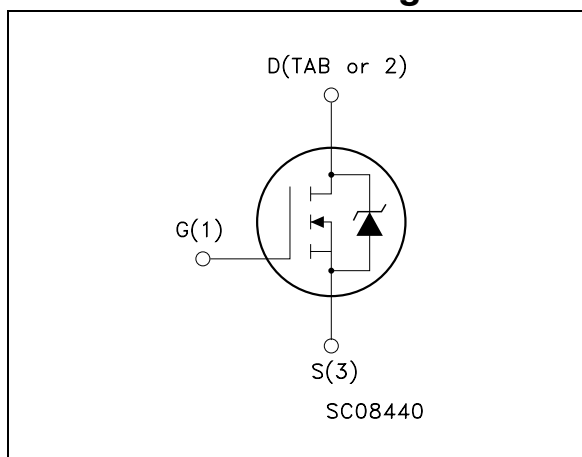
This MOSFET is the latest refinement of STMicroelectronic unique “Single Feature Size™” strippbased process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics, low gate charge and less critical alignment steps therefore a remarkable manufacturing reproducibility. This new improved device has been specifically designed for Automotive application and DC-DC converters.

## Applications

- Switching application



## Internal schematic diagram



## Order codes

Part number	Marking	Package	Packaging
STD100N03LT4	D100N03L	DPAK	Tape & reel
STD100N03L-1	D100N03L-1	IPAK	Tube

# Contents

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	30	V
$V_{DGR}$	Drain-gate voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	80	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	70	A
$I_{DM}^{(2)}$	Drain current (pulsed)	320	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$	110	W
	Derating factor	0.73	W/ $^\circ\text{C}$
$dv/dt^{(3)}$	Peak diode recovery voltage slope	3.9	V/ns
$T_{stg}$	Storage temperature	-55 to 175	$^\circ\text{C}$
$T_J$	Max. operating junction temperature		

1. Current limited by package.
2. Pulse width limited by safe operating area
3.  $I_{SD} \leq 80\text{A}$ ,  $di/dt \leq 360\text{ A}/\mu\text{s}$ ,  $V_{DS} \leq V_{(BR)DSS}$ ,  $T_J \leq T_{JMAX}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance junction-case Max	1.36	$^\circ\text{C}/\text{W}$
$R_{thJA}$	Thermal resistance junction-ambient Max	100	$^\circ\text{C}/\text{W}$
$T_I$	Maximum lead temperature for soldering purpose	275	$^\circ\text{C}$

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Not-repetitive avalanche current (pulse width limited by $T_J$ max)	40	A
$E_{AS}$	Single pulsed avalanche energy (starting $T_J = 25^\circ\text{C}$ , $I_D = I_{AV}$ , $V_{DD} = 24\text{V}$ )	500	mJ

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu A, V_{GS} = 0$	30			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating},$ $V_{DS} = \text{Max rating} @ 125^{\circ}C$			1 10	$\mu A$ $\mu A$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20V$			$\pm 200$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 40A$ $V_{GS} = 5V, I_D = 20A$		0.0045 0.008	0.0055 0.01	$\Omega$ $\Omega$
		$V_{GS} = 10V,$ $I_D = 40A @ 125^{\circ}C$ $V_{GS} = 5V,$ $I_D = 20A @ 125^{\circ}C$		0.0068 0.0146		$\Omega$ $\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 10V, I_D = 15A$		31		S
$C_{iss}$	Input capacitance	$V_{DS} = 25V, f = 1\text{ MHz},$ $V_{GS} = 0$		2060		pF
$C_{oss}$	Output capacitance			728		pF
$C_{rss}$	Reverse transfer capacitance			67		pF
$Q_g$	Total gate charge	$V_{DD} = 24V, I_D = 80A$		20	27	nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 5V$		7		nC
$Q_{gd}$	Gate-drain charge	<a href="#">Figure 15 on page 9</a>		7.5		nC
$R_G$	Gate input resistance	$f = 1\text{ MHz gate DC Bias} = 0$ Test signal level = 20mV Open drain		1.9		$\Omega$

1. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15V, I_D = 40A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ <i>Figure 14 on page 9</i>		9		ns
$t_r$	Rise time			205		ns
$t_{d(off)}$	Turn-off delay time			31		ns
$t_f$	Fall time			35		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current				80	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				320	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 40A, V_{GS} = 0$			1.3	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 80A,$ $di/dt = 100A/\mu s,$ $V_{DD} = 25V, T_J = 150^\circ C$ <i>Figure 16 on page 9</i>		40		ns
$Q_{rr}$	Reverse recovery charge			40		$\mu C$
$I_{RRM}$	Reverse recovery current			2		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

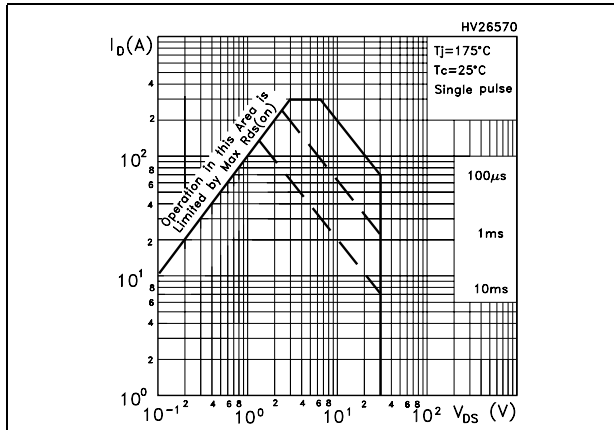


Figure 2. Thermal impedance

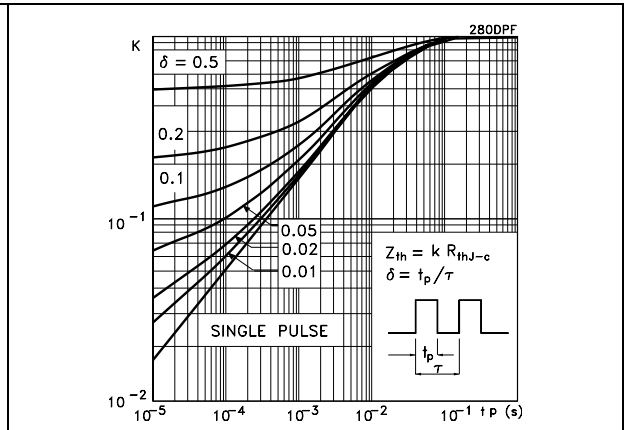


Figure 3. Output characteristics

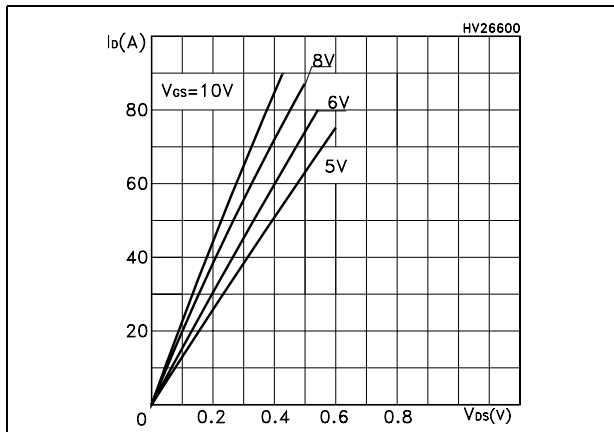


Figure 4. Transfer characteristics

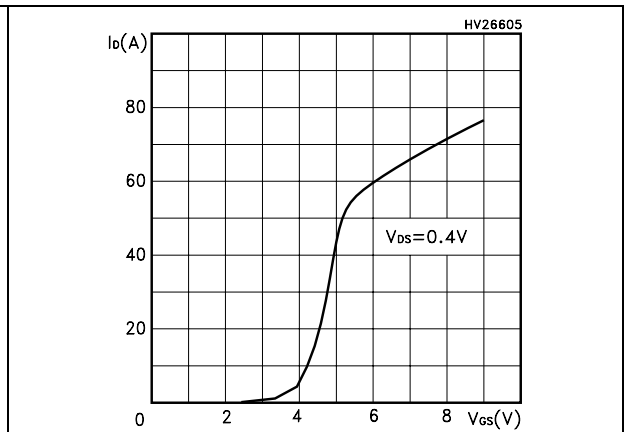


Figure 5. Transconductance

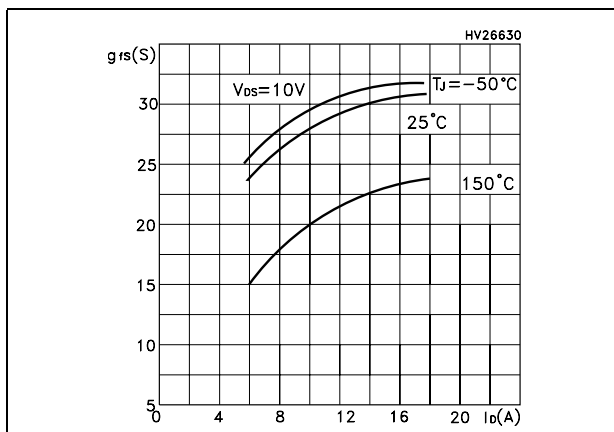


Figure 6. Static drain-source on resistance

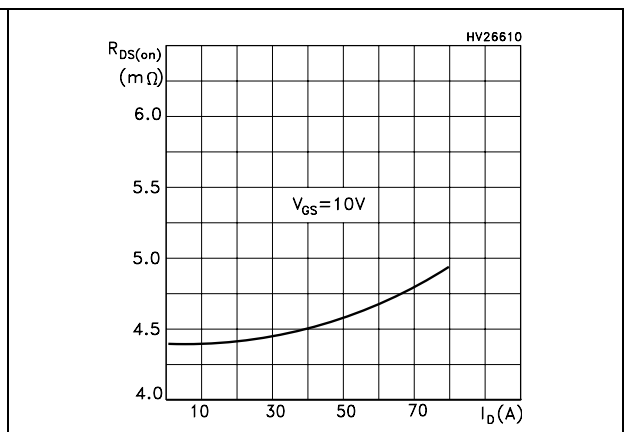


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

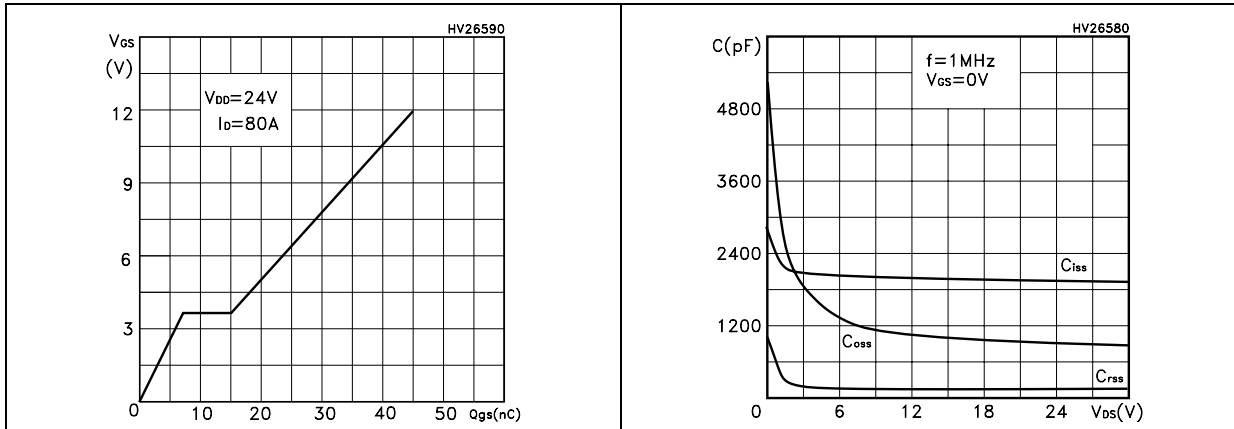


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized BVDSS vs temperature

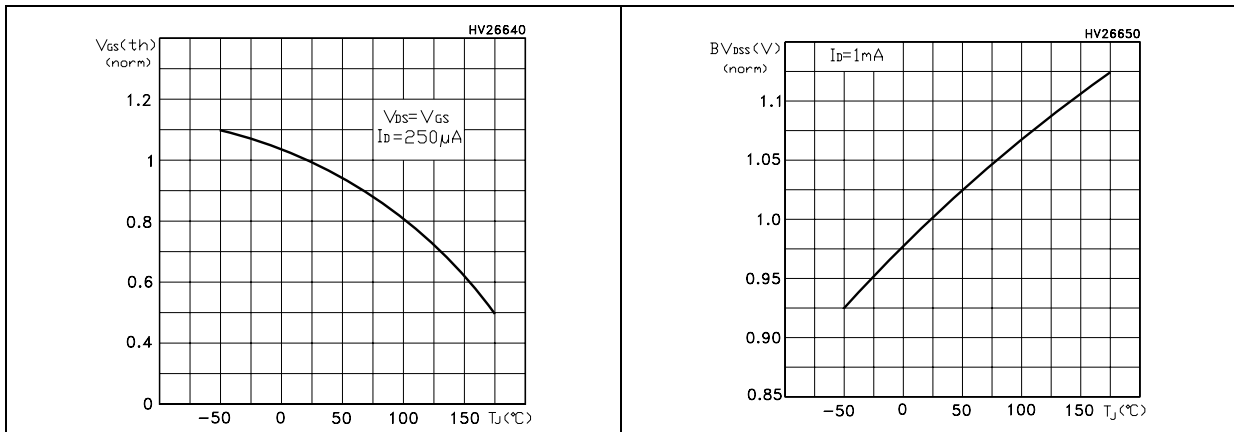


Figure 11. Normalized on resistance vs temperature Figure 12. Source-drain diode forward characteristics

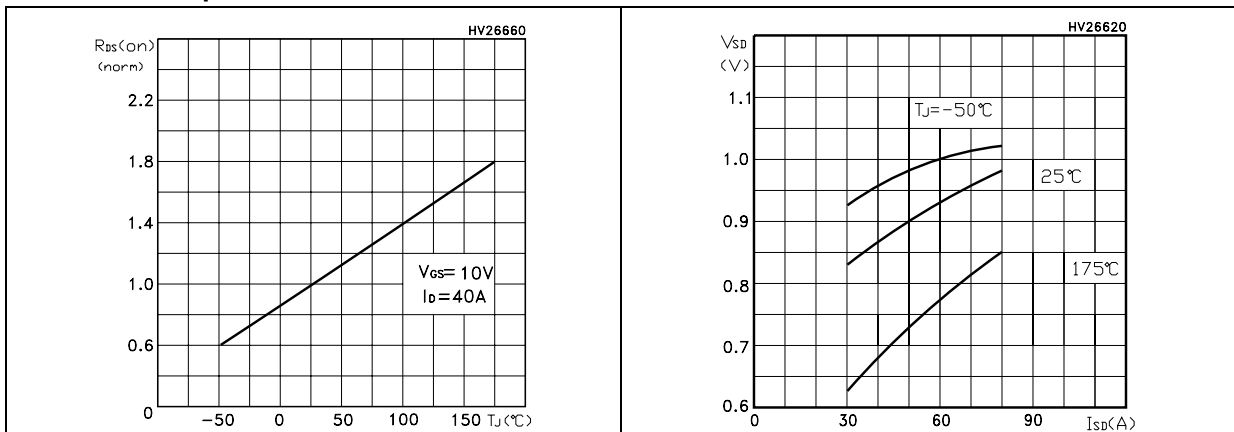
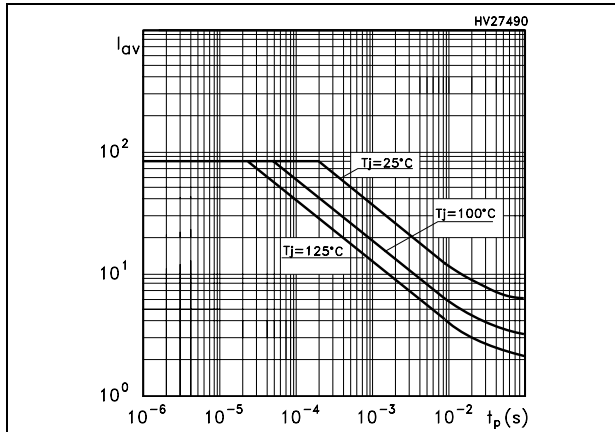


Figure 13. Allowable  $I_{AV}$  vs time in avalanche



The previous curve gives the single pulse safe operating area for unclamped inductive loads, under the following conditions:

$$P_{D(AVE)} = 0.5 * (1.3 * BV_{DSS} * I_{AV} )$$

$$E_{AS(AR)} = P_{D(AVE)} * t_{AV}$$

Where:

$I_{AV}$  is the Allowable Current in Avalanche

$P_{D(AVE)}$  is the Average Power Dissipation in Avalanche (Single Pulse)

$t_{AV}$  is the Time in Avalanche



### 3 Test circuit

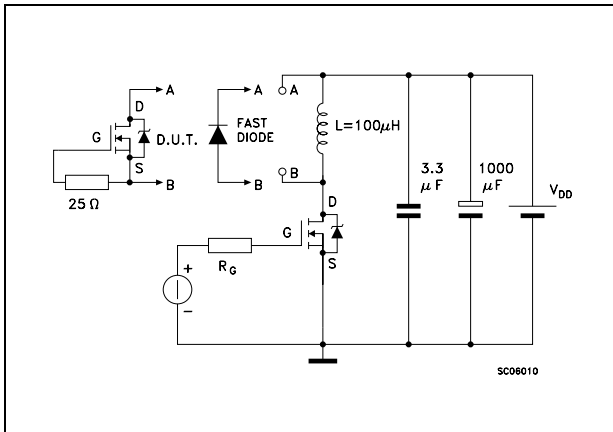
Figure 14. Switching times test circuit for resistive load



Figure 15. Gate charge test circuit



Figure 16. Test circuit for inductive load switching and diode recovery times

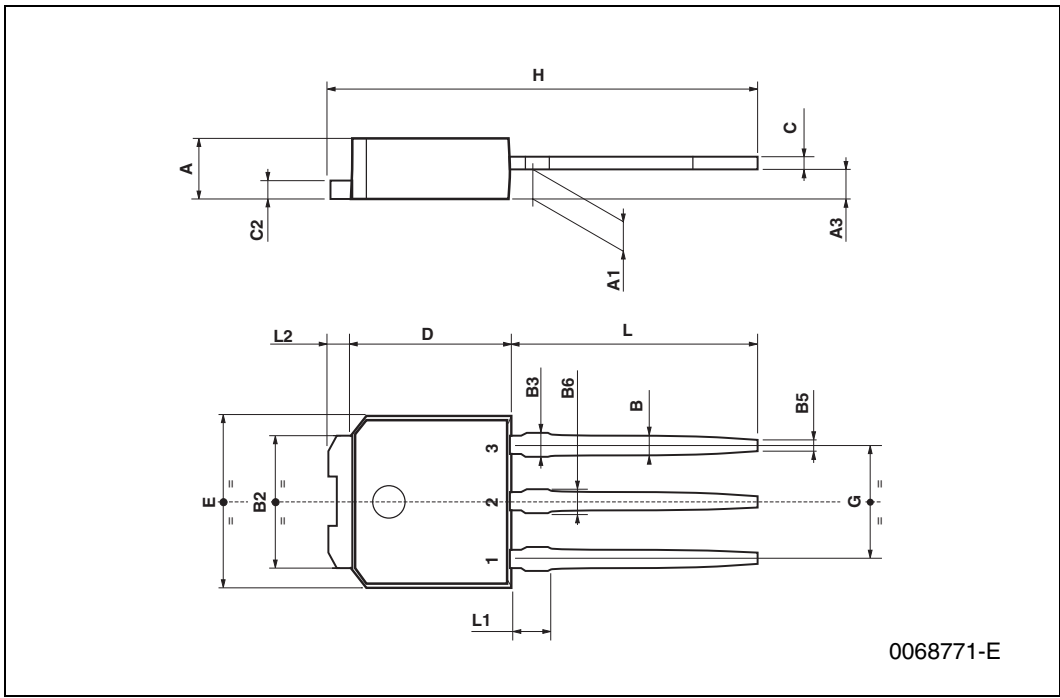


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

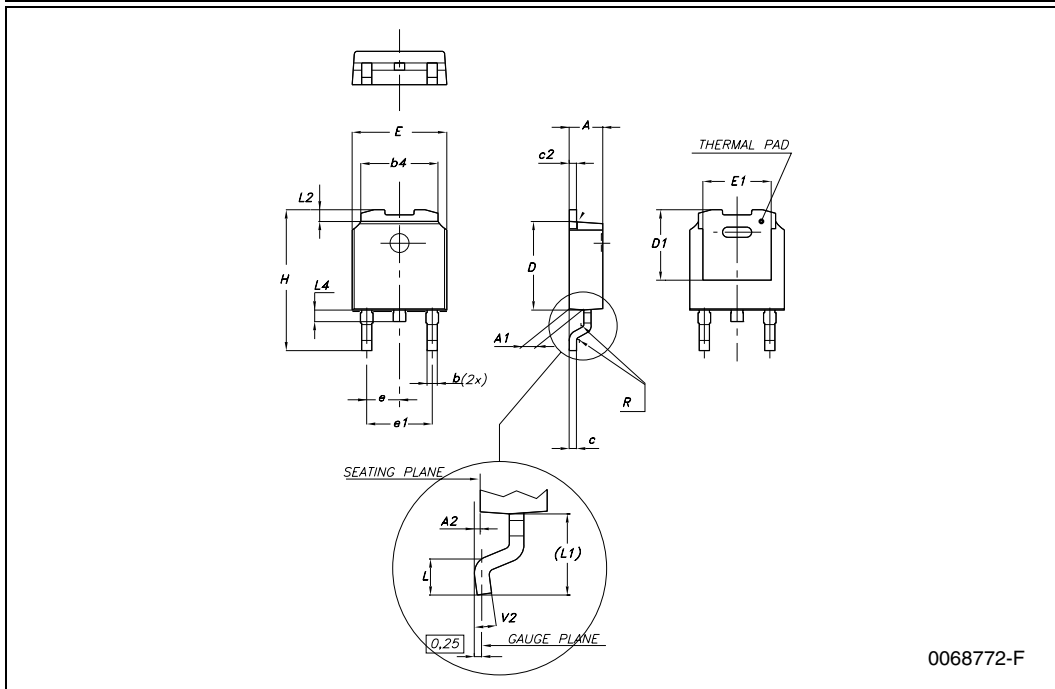
**TO-251 (IPAK) MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



**DPAK MECHANICAL DATA**

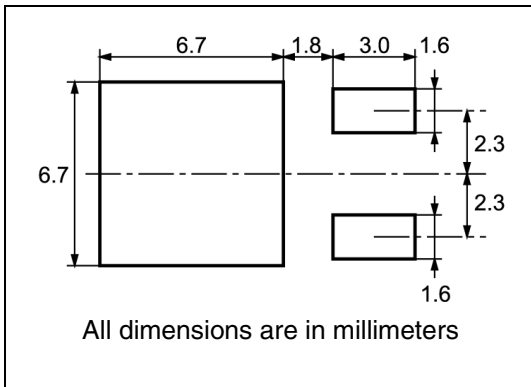
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°



0068772-F

# 5 Packaging mechanical data

## DPAK FOOTPRINT



## TAPE AND REEL SHIPMENT

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

## 6 Revision history

**Table 8. Revision history**

Date	Revision	Changes
15-Sep-2005	1	Initial release.
14-Sep-2005	2	Value changed on <i>Figure 1</i>
08-Aug-2006	3	New template, no content change

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